What is Claimed is:

1. A method of manufacturing a semiconductor device comprising the steps of:

forming a gate insulating layer on a semiconductor substrate;

forming a silicon gate layer on said gate insulating layer;

forming gate lines by patterning said silicon gate layer;

performing an impurity implantation by using said gate lines as a mask;

forming an interlayer insulating layer over said substrate over which said impurity implantation is carried out;

exposing said silicon gate layer of said gate lines by planarizing said interlayer insulating layer; and

forming a metal silicide layer on an exposed surface of said silicon gate layer.

2. The method of manufacturing a semiconductor device according to claim 1, further including the steps of forming openings to expose a given region of said substrate by partially etching said interlayer insulating layer after said step of forming said interlayer insulating layer, and filling said openings by depositing a silicon layer; and

wherein said step of exposing said silicon gate layer of said gate lines includes planarizing said silicon layer.

3. The method of manufacturing a semiconductor device according to claim 1, wherein said step of forming said metal silicide layer comprises:

depositing a metal layer by a sputtering process;

annealing said metal layer; and

removing non-reacted residual metal by an etching process.

4. A method of forming a cell area of a flash memory device comprising the steps of:

forming an active region having a plurality of line shaped sub-regions on a semiconductor substrate, each being defined parallel to each other by an isolation layer;

forming a gate insulating layer and a silicon floating gate layer in said active region;

forming a floating gate intermediate pattern by patterning said floating gate layer;

forming a dielectric layer over the whole surface of said substrate over which said floating gate intermediate pattern is formed;

forming a silicon control gate layer over said substrate over which said dielectric layer is formed;

forming a plurality of gate lines in a direction vertical to a direction forming said active region by etching partially said silicon control gate layer, said dielectric layer, and said floating gate intermediate pattern;

doping said active region between said gate lines by using a dose of impurity below 1.0×10^{15} ions/ cm^2;

forming a lower interlayer insulating layer over the whole surface of said substrate over which said doping is carried out;

forming a groove exposing a common source region in said active region by etching partially said lower interlayer insulating layer;

depositing a silicon layer to fill said groove;

forming a wall shaped silicon common source line with exposing upper portions of said gate lines by planarizing said silicon layer and said lower interlayer insulating layer; and

forming a metal silicide layer on exposed upper surfaces of said gate lines and said silicon common source line.

5. The method of forming a cell area of a flash memory device according to claim 4, further including the step of forming an etch stop layer over the whole surface of said substrate between said step of doping and said step of forming said lower interlayer insulating layer.

6. The method of forming a cell area of a flash memory device according to claim 4,

wherein said step of forming said groove includes forming contact holes in bit line contact regions; and

further including the steps of:

forming an upper interlayer insulating layer after said step of forming said metal silicide layer;

forming contact holes in said bit line regions by etching partially said upper interlayer insulating layer;

depositing a wiring metal layer for bit lines and bit line contacts; and

forming bit lines by patterning said wiring metal layer.